

ACQUISITION AID CIRCUIT

Abstract of the Disclosure

5 The invention relates to methods and apparatus that compare the frequencies of a first clock signal and a second clock signal and reliably provide an indication of whether the frequency relationship between the first clock signal and the second clock signal is within a predetermined range. In one embodiment, the first clock signal is a reference clock signal and the second clock signal is generated from a serial bitstream. The indication can be used to synchronize a voltage controlled oscillator within a phase locked loop to the reference clock signal to thereby keep the phase locked loop within a lock range of a serial bitstream from which the second clock is generated. Embodiments of the invention digitally generate a beat frequency related to a difference in speed between the first clock signal and the second clock signal. The beat frequency is synchronized, advantageously obviating the need to synchronize asynchronous counters as is conventionally done.

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